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Semiconductor Technology Program Progress Briefs

W. Murray Bullis, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
U.S. Department of Commerce
Washington, D.C. 20234

June 1980

Prepared for

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The Division of Distributed Solar Technology, Department of Energy
The Defense Nuclear Agency
The Charles Stark Draper Laboratory
The Naval Air Systems Command
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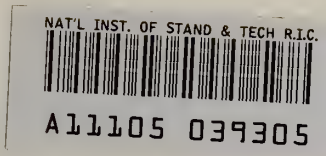

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SEMICONDUCTOR TECHNOLOGY PROGRAM

TABLE OF CONTENTS

MOSFET dc Profiler 3

Heavy Doping Effects in Silicon 3

PVW Applications 3

Ion-Implanted Profiles 4

Optical Linewidth Measurements 5

Transistor Switching Characteristics . . 6

Process-Induced Radiation Damage 7

Acoustic Emission Testing 8

Work in Progress 8

Recent Publications 9

Publications in Press 10

ABSTRACT — This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: studies of MOSFET dc profiler, heavy doping effects in silicon, PVW applications, ion-implanted dopant profiles, optical linewidth measurements on wafers, process-induced radiation damage, transistor switching characteristics, and acoustic emission testing. Brief descriptions of selected on-going projects are included, and recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

KEY WORDS — Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the forty-seventh quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Distributed Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Naval Air Systems Command; 8. The Air Force Wright Aeronautical Laboratories; 10. The Naval Weapons Support Center; 11. The Solar Energy Research Institute; 12. The Naval Avionics Center; 13. The Lewis Research Center, National Aeronautics and Space Administration; 14. The Office of Naval Research; and 15. The Naval Ocean Systems Center.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

MOSFET dc Profiler

As part of a study aimed at characterizing a variety of buried-layer implants under simulated CCD processing steps, a MOSFET dc profiler was used to profile four different ion implants of the type used for radiation-hardened, buried-channel CCD imagers. The purpose of the study is to obtain data which may lead to an implant schedule which will yield greater CCD radiation tolerance without sacrificing full-well capacity. The profiler is a rectangular MOSFET with a channel length of 28 μm, fabricated on an n-type <111> silicon wafer with nominal room-temperature resistivity of 10 Ω·cm.

Two wafers were implanted with phosphorus at 140 keV to a fluence of 1.5 x 10^{12} or 3 x 10^{12} cm^{-2} through an oxide approximately 10 nm thick to randomize the distribution of the implanted ions. The overall agreement between the results obtained from the two profiling methods is generally quite good; but there are some systematic differences. A more detailed analysis is being made. [Sponsor: 2]

(G. P. Carver, x3541, and J. R. Ehrstein, x3625)

Heavy Doping Effects in Silicon

A study was completed of the disappearance of shallow donor impurity levels in silicon and germanium at large dopant densities which results from free-carrier screening of the impurity ions. The ground state eigenfunctions and eigenvalues were calculated for electrons described by an ellipsoidal effective-mass Hamiltonian in the screened Coulomb field of an isolated donor impurity atom. An extreme case in which the longitudinal-to-transverse effective-mass ratio is 100:1 was also considered. The solutions were obtained with the use of a two-dimensional finite-element analysis which includes adaptive mesh procedures. Particular care was taken to assure that there is no addition of electron states to the total number associated with the perfect crystal. The study was restricted to donors because the valence band is degenerate, and therefore the mathematics associated with shallow acceptor impurity levels is more complex.

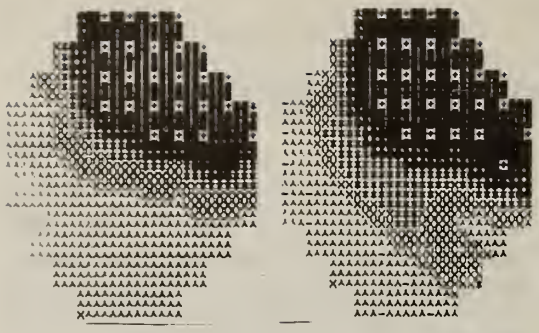
The results show that the donor level moves closer in energy to the conduction band with increasing donor density. Only moderate carrier densities ($\sim 10^{19}$ cm^{-3} for silicon and $\sim 10^{18}$ cm^{-3} for germanium) at room temperature are needed to cause the impurity levels to completely disappear into the conduction band. It is concluded that a more heavily doped, essentially uncompensated semiconductor should be treated as simply degenerate with appropriate account taken of the band distortions which are due to the interactions of the conduction electrons with the screened impurity ions as well as with each other. Inclusion of a distinct impurity band at high dopant densities, which has the effect of pinning the Fermi energy within the forbidden gap, is not correct. [Sponsor: 2]

(J. R. Lowney and C. L. Wilson, x3625, A. H. Kahn,* and J. L. Blue†)

PVW Applications

The test results from a process validation wafer (PVW) were successfully uti-

*NBS Ceramics, Glass, and Solid State Science Division.
†NBS Scientific Computing Division.



Wafer maps showing correlation between metal-to-n^+ contact resistance (left) and sheet resistance of the n^+ layer (right). Darker symbols represent larger values.

lized to identify an unsuspected problem affecting wafer fabrication process control in a radiation-hardened silicon-gate CMOS/SOS process at a commercial manufacturer. The PVW contained test pattern NBS-16 replicated at 95 sites on the wafer. This test pattern contains a wide variety of parametric test structures, including MOSFETs, contact resistors, cross-bridge sheet resistors, and capacitors, in addition to random fault test structures.

Test results from 18 PVWs indicated a wide range in the magnitude of metal-to-n^+ contact resistance from lot to lot and across a wafer. Very little variation in the metal-to-p^+ contact resistance was observed indicating that the problem was not a function of the contact-window photolithography process. Wafer maps of metal-to-n^+ contact resistance and n^+ sheet resistance for the PVW accompanying one of the wafer lots are seen in the accompanying figures. The approximate correlation between the two maps suggests that the cause of high metal-to-n^+ contact resistance was a low phosphorus concentration at the silicon surface. This surface concentration was controlled by a phosphorus implant through the gate oxide layer into the source and drain regions of the epi island. Subsequent testing of MOS capacitors indicated that the gate oxide was thicker in the areas of lowest phosphorus concentration. It was concluded that variations in the gate oxide thickness caused the peak of the phosphorus implant to vary between the silicon and silicon dioxide, which in turn resulted in significant variations in the number of phosphorus atoms reaching the silicon surface and caused the observed variation in metal-to-n^+ contact resistance. It was possible to solve this problem by increasing the accelerating potential of the implant to reduce the effect of gate oxide thickness on the number of phosphorus atoms which reach the silicon. [Sponsor: 8]

(L. W. Linholm, x3541)

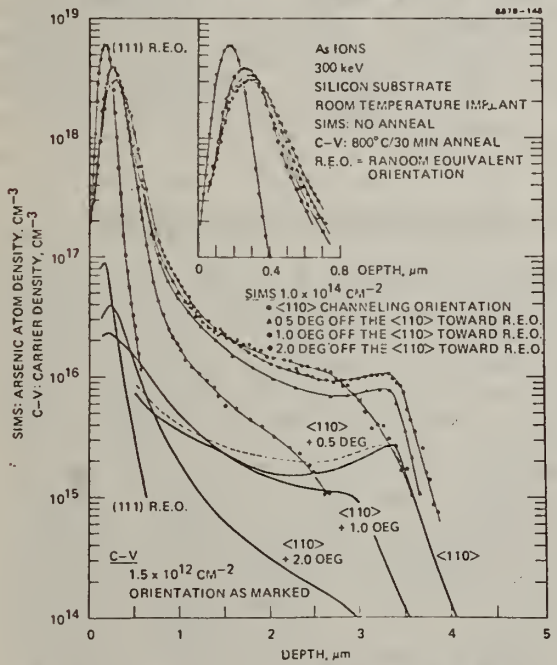
Ion-Implanted Profiles

Atom depth distributions for arsenic channeled deeply in the <110> direction of a silicon crystal, measured by secondary ion mass spectrometry (SIMS), show agreement with carrier depth distributions previously measured for similar (but lower fluence) 300-keV arsenic-channeled implants by differential capacitance-voltage (C-V) profiling techniques. The silicon wafers were cut from 100-Ω·cm float-zoned crystals with (110) faces. The arsenic was implanted at several angles with respect to the <110> crystallographic direction: accurately aligned (within ∿0.05 deg of the <110> axis, for maximum axial channeling) and 0.50, 1.00, and 2.00 deg away from the <110> axis in a direction toward a random equivalent orientation (REO). Alignment angles were measured by Rutherford backscattering.

The atom depth distributions were measured using a cesium ion beam and by recording the secondary positive ions at mass 75. The SIMS crater depths were measured using a surface profilometer. The atom densities were determined by equating the integrals of the depth distributions to the implantation fluences. The excellent background-subtracted detection limit of 1×10^{15} cm^{-3} for arsenic in silicon was instrumental in obtaining the results reported here.

The carrier depth distributions were measured by differential capacitance-voltage techniques on 125-μm diameter gold Schottky barrier diodes. The use of 100 Ω·cm float-zoned silicon was responsible for the detection limit of about 1 x 10^{14} cm^{-3} for the carrier profiles. The estimated error in both the SIMS and C-V depth scales is ±10%; however, the agreement found between the two different techniques suggests a smaller error.

The results are illustrated in the accompanying figure. These results show that the atom depth distributions of arsenic channeled in the <110> direction of silicon can be measured by SIMS, that these depth distributions and those of the associated carriers measured by differential C-V profiling are similar in shape and both give a most probable channeling range at the peak of the channeled distribution of 3.35 to 3.40 μm and a maximum channeling range of about 4.0 μm for the 300-keV ion energy, that the saturated or maximum arsenic atom density achievable under these conditions is ∿1.5 x 10^{16} cm^{-3}, that no significant redistribution of channeled arsenic atoms occurs upon annealing at 800°C for 30 min, that little if any degradation of the channeled profile occurs for 0.50-deg misalignment from the <110> direction of silicon, and that significant degradation, as measured by both SIMS (atom density) and C-V (associated carrier distribution), occurs for misalignment angles of 1.0 and 2.0 deg. [Sponsor: 1] (D. R. Myers,* x3625)



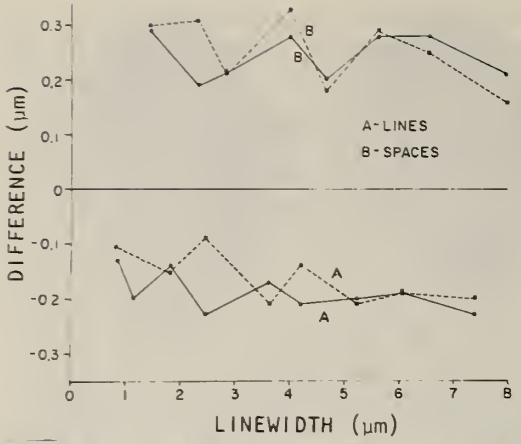
Depth distributions of atoms measured by SIMS and of associated carriers measured by differential C-V for 300-keV arsenic ions channeled in the <110> direction of a silicon lattice as a function of alignment angle.

Optical Linewidth Measurements

In contrast to earlier work with nearly opaque photomasks, optical linewidth measurements on wafers encompass materials with a much wider variation in optical parameters and material profiles. Accurate optical edge detection requires corrections for both the relative reflectance and phase at the line edge because of the partial coherence present in optical microscopes used for linewidth measurements. However, measurement systems which cannot provide the appropriate corrections and cannot detect edge location accurately can be calibrated, provided that the repeatability of the measurement is satisfactory.

The NBS reflected light scanning photometric microscope was used to calibrate a wafer made by contact printing an antireflective chromium mask onto a 150-nm thick layer of silicon dioxide on silicon. The wafer was plasma etched to get the steepest possible material edges. The pattern contained linewidths between 0.5 and 11 μm with both polarities. This wafer was then measured on a variety of commercially available linewidth measurement systems. In each case, the

*NBS contact; work carried out by R. G. Wilson, H. L. Dunlap, D. M. Jamba, and P. K. Vasudev of Hughes Laboratories and V. R. Deline and C. G. Hopkins of Charles Evans and Associates.



Difference (measured values minus NBS values) for filar (dashed) and image-shearing (solid) systems vs. NBS laser linewidth measurements. Filar and image-splitting systems used center of dark band at the line edge for measurement. These data apply only to a 150-nm thick etched silicon dioxide layer.

optical microscope was set up following the NBS-recommended procedures for photomasks which includes the use of Kohler illumination, a coherence parameter R of 2/3, and broadband green (WR60) spectral illumination.

Measurements were made with an optical filar eyepiece (dashed crosshair), a coincidence-setting image-shearing system with video display, two types of photometric scanning systems using different edge detection methods, and a video image-scanning system. The results for the first two of these systems are shown in the accompanying figure. The principal effect illustrated is the polarity-dependent edge detection error expected from use of the center of the dark interference band to determine the edge location. In both cases, the data could be used as calibration data to correct for this known systematic error.

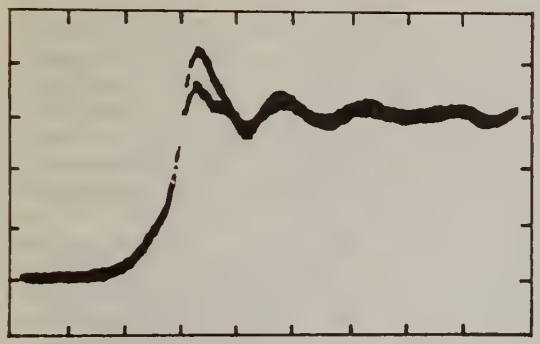
In principle, since the calibration curve is material dependent, a calibration curve is required for each material and each thickness corresponding to each step in the wafer fabrication process where linewidth measurements are made. However, it is not feasible to provide calibration wafers for, or calibrate, linewidth measurement systems for all combinations of relative reflectance and phase for all materials of interest. An alternative approach is to supply a small number of calibration wafers and calibrate the system using the one which most closely matches the unknown in relative reflectance and phase. The maximum possible error would be known and a correction could be applied if the relative reflectance and phase of the unknown were measured. The accuracy of this proposed calibration method is dependent upon the predictability and precision of the calibration curves for a given instrument and remains to be determined for systems in use in the IC industry.

Details of this work were presented at the S.P.I.E. Seminar on Developments in Semiconductor Lithography V in March and will appear in volume 221 of the S.P.I.E. *Proceedings*. [Sponsors: 2,7]

(D. Nyyssonen, J. M. Jerke, and D. B. Novotny, x3621, and Y. M. Liu, x3541)

Transistor Switching Characteristics

When a transistor which has an inductive load at its collector terminal begins to turn off, the voltage at the collector rises as the inductor attempts to maintain a constant current. For high voltage, fast switching transistors, the voltage can rise rapidly, perhaps as much as 500 V in 100 ns. In most applications, the maximum voltage rise is limited by a voltage clamping circuit connected to the collector. Usually, the voltage clamp consists of a semiconductor diode in series with a voltage source (clamp voltage) arranged in such a manner that the bias on the diode is equal to the difference between the collector voltage and source voltage. When the collector voltage is lower than the clamp voltage, the diode is reverse biased. When the collector voltage rises slightly above the clamp voltage, the



Oscilloscope traces of voltage overshoot using a clamp circuit with a semiconductor diode or a vacuum tube diode. The vertical scale is 100 volts per division; the horizontal scale is 50 nanoseconds per division. The overshoot is about 100 V for the semiconductor diode, about 50 V for the vacuum diode.

diode is forward biased, the current is shunted from the transistor, and the collector voltage is limited to the clamp voltage less the relatively small voltage drop across the diode.

The response characteristics of the diode are such that a finite time (∿50 ns) is required for even the fastest semiconductor diodes which can handle the power levels involved to switch from a reverse-bias condition to a forward-bias condition. This results in an overshoot of the collector voltage above the clamp voltage for a time comparable with the reverse recovery time of the diode. The overshoot has been observed to be over 100 V for some very fast bipolar transistors tested on the NBS second-breakdown test circuit. Because of the overshoot, these very fast devices appear to experience second breakdown at lower clamp voltages than they would if no overshoot occurred.

To reduce the overshoot, the semiconductor diodes in the NBS circuit were replaced with vacuum tube diodes (6CG3) which, because they have no charge storage, assume their conducting state much more rapidly than the semiconductor diodes. The result has been to eliminate overshoot in some instances and substantially reduce it in others. The accompanying figure illustrates a worst case condition where the overshoot reduction is 50%. The remaining overshoot is due to inductance.

The vacuum diode clamp has two disadvantages. First, it has a voltage drop (∿45 V at 10 A) substantially larger than that of the semiconductor diode; this can be corrected for in establishing and recording the clamp voltage. Second, it introduces an increased parasitic capacitance at the collector of the device being tested. The effect of this increased capacitance on the second-breakdown characteristics of the device being tested has not been fully determined. Therefore, the vacuum diode clamp is only used when the voltage overshoots are a problem; at other times, the semiconductor diode clamp is used. [Sponsor: 13]

(D. W. Berning, x3621)

Process-Induced Radiation Damage

Estimates have been made of the radiation dose absorbed in critical device dielectric layers during the application of ion-beam lithography (IBL) to facilitate comparison of this technique with other lithographic techniques delivering a radiation dose to device structures during processing. Calculations were made for a typical structure in which a silicon substrate is covered by a 0.05-μm thick film of silicon dioxide which is covered by a 1.0-μm thick film of aluminum or polysilicon which is in turn covered with a 1.0-μm thick film of photoresist to be patterned by IBL.

The results indicate that although 200-keV protons at a fluence of 2×10^{13} cm^{-2} can deposit several hundred megarads* into the oxide through the aluminum or polysilicon, the radiation absorbed dose in critical oxide layers can be essentially eliminated by carefully

*The Si unit for absorbed dose is the gray (Gy) which is equivalent to one joule per kilogram; 1 Gy = 100 rad.

matching the ion beam energy to the material configuration. In general, this means operating with a beam energy which is as low as practicable after accounting for mask membrane penetration and allowing for loss of resolution due to beam scattering and which is high enough to achieve uniform exposure and minimize lateral scattering in the resist. This ability to reduce the radiation absorbed dose in the oxide may provide a significant advantage over electron-beam or x-ray lithography. [Sponsor: 2]

(K. F. Galloway, x3625)

Acoustic Emission Testing

In a study to evaluate the use of acoustic emission monitoring of glass-to-metal seals in hybrid packages during temperature cycling from -55° to 125°C, an acoustically quiet temperature cycling system is essential to avoid interference with the signals from the seals. A thermoelectric temperature cycling system was investigated because it was expected that such a system would be acoustically quiet. However, it was observed that the thermoelectric modules themselves emitted large bursts of acoustic emission, especially when they were cooling.

A series of experiments was conducted to determine the origins of the acoustic emission bursts. The results of these experiments suggested that twinning or other crystallographic changes occurred in the bismuth telluride elements as a result of rapid temperature changes.

In addition, several thermoelectric modules that had been cycled more than 1000 times and had become inefficient on the cooling cycle were visually examined around their bismuth telluride element solder joints. Microcracks were observed in the solder, and surface reconstruction of the solder was evident indicating that recrystallization had taken place. Also, some cracks were observed in the bismuth telluride elements.

As a consequence of these results, it does not appear possible to use thermoelectric temperature cycling equipment in electronic or other applications that require acoustic emission monitoring. It should be noted that most of the thermoelectric module degradation processes, such as cracks, are considered to result from the large range of the temperature cycling. Thermoelectric modules are generally used only for cooling from room temperature, and crack propagation and solder reconstruction would probably not occur in this temperature range. Twinning of the bismuth telluride should not degrade the performance of the cooling modules. [Sponsors: 12,2] (G. G. Harman, x3621)

Work in Progress . . .

Gross Leak Testing — Further tests were carried out to determine why the leak rate as measured by the two-chamber mode of the rapid cycle leak test was larger than predicted for leak sizes in the range from about 2×10^{-5} atm·cm^3/s to about 4×10^{-5} atm·cm^3/s. The original model assumed laminar viscous flow; the model was extended to include mixed flow through the leak channels to determine if other flow mechanisms become significant at these relatively small gross leak sizes. However, agreement with experimental results was not obtained with the mixed-flow model. Since the measurements in question were near the threshold capability, further studies were carried out to reevaluate the background leak rate for these test capsules. The results showed that the earlier reference capsule gave anomalously low sorption effects; data corrected to the proper background level conform to theory at the small values. [Sponsor: 2] (S. Ruthberg, x3621)

Carbon in Silicon — It was demonstrated that the distribution of carbon in a silicon wafer can be measured with adequate sensitivity and with a 1-mm spatial resolution using a Fourier trans-

form infrared spectrometer. An x-ray topography station is being set up to study the carbon-induced strain in the silicon lattice. It is expected that the spatially resolved infrared measurements will facilitate correlation of the carbon density distribution with x-ray topography data. [Sponsor: 2]

(A. Baghdadi, x3625)

Analysis of C-V Profiles — A new, high accuracy, finite-element method is being used to calculate capacitance-voltage curves for dopant profiles which are piecewise approximated by up to 200 exponential segments. An incremental charge approach is used to calculate the capacitance; use of the depletion approximation is avoided. This procedure has been extended to allow profile calculation using self-consistent iteration. An initial profile deduced from the measured C-V data (using the classical Schottky equation) is input to an exact numerical calculation of the C-V characteristic. This characteristic is then iteratively improved by correcting the doping profile directly. This correction procedure provides two to five times the resolution of the uncorrected procedure. [Sponsor: 2]

(C. L. Wilson, x3625)

Unintentional Channeling During Ion Implantation — A study is nearing completion of the effects of surface oxide layer thickness on the implantation profiles of boron implanted into (100)-oriented silicon at 0-deg tilt. The through-the-oxide configuration is customarily employed in order to randomize the implant profile. This study was motivated by two trends which have recently evolved in ion implantation for silicon device fabrication: implantation at 0-deg tilt to improve uniformity for large diameter wafers, and the use of thinner gate oxides to satisfy device scaling rules. Boron was implanted into (100) silicon at 0.0 $\pm$ 0.1 deg through various thicknesses of thermally grown silicon dioxide. The implants were performed at room temperature at 150 keV to a fluence of 4.0×10^{13} cm^{-2}. The oxide surface layers examined were 8, 34, 101, or 140 nm thick, as determined by ellipsometry. The boron profiles were determined by secondary ion mass spectrometry. The boron profile for implantation through an 8-nm oxide surface layer was only slightly degraded from that seen for accurately aligned implantations into bare (100)-oriented silicon, while implantation through oxides 34 nm thick or greater resulted in profiles similar to those obtained from random equivalent implantations into crystalline silicon. Work is proceeding to evaluate existing analytic theories on the basis of these results. [Sponsors: 1,2]

(D. R. Myers,* x3625)

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*J. Comas, Naval Research Laboratory, and R. G. Wilson, Hughes Research Laboratories, also contributed to this work. Dr. Comas' research was supported in part by the Office of Naval Research.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: studies of MOSFET dc profiler, heavy doping effects in silicon, PVW applications, ion-implanted dopant profiles, optical linewidth measurements on wafers, process-induced radiation damage, transistor switching characteristics, and acoustic emission testing. Brief descriptions of selected on-going projects are included, and recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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